RINGKASAN

ANALISIS PENGARUH OVERLAP TIME PADA UNJUK KERJA CURRENT SOURCE INVERTER MULTILEVEL

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Open circuit merupakan kondisi dimana rangkaian terputus yang mengakibatkan arus dari sumber tidak mengalir menuju beban. Open circuit dalam inverter sumber arus merupakan kondisi yang harus dihindari. Hal ini karena kondisi tersebut akan menghasilkan tegangan tinggi yang dapat merusak komponen penskalaran. Oleh karena itu, perlu dilakukan penambahan rangkaian overlap guna memberikan waktu tunda outgoing saklar (saklar yang telah aktif) ketika beralih dari posisi ON ke OFF sehingga akan terjadi overlap (tumpang tindih antara saklar yang akan aktif dan saklar yang telah aktif). Hal ini untuk memastikan bahwa saklar yang akan aktif telah ON ketika outgoing saklar dalam posisi OFF.

Pada penelitian ini, dilakukan variasi overlap time pada inverter sumber arus multilevel. Variasi ini diperlukan agar dapat dianalisis bagaimana pengaruh overlap time pada unjuk kerja CSI multilevel. Selain itu, dalam penelitian ini akan dijelaskan bagaimana meminimalisir efek negatif yang ditimbulkan oleh penambahan overlap time pada CSI multilevel. Pada pengujian overlap time CSI multilevel diberikan variasi overlap time dari 0 us hingga 5 us. Pada pengujian ini didapat bahwa semakin besar overlap time yang digunakan, semakin besar nilai THD dari arus keluaran inverter.

Adapun untuk meminimalisir efek negatif dari pemberian overlap time, diberikan suatu kompensasi overlap time. Terdapat 2 metode dasar sebagai kompensasi yakni menggunakan total carrier segitiga dan menggunakan setengah dari total carrier segitiga. Selain itu digunakan pula metode kedua namun dengan beda fase antar segitiga sebesar 180. Pada masing-masing puncak bawah dari segitiga, diperpanjang sesuai besar kompensasi. Sehingga puncak bawah dari segitiga tersebut melewati DC offset semula dan mengcross-over segitiga yang ada dibawahnya. Dari metode-metode digunakan, metode dengan menggunkan setengah dari total carrier segitiga sangat efektif meminimalisir efek negatif dari pemberian overlap time yakni dapat menurunkan nilai THD dari gelombang keluran inverter.

Kata kunci : *Overlap Time, Current Source Inverter Multilevel, Open Circuit*

SUMMARY

OVERLAP TIME EFFECT ANALYSIS ON MULTILEVEL CURRENT SOURCE INVERTER PERFORMANCE

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Open circuit is a condition where the circuit is interrupted which causes the current from the source not to flow towards the load. The open circuit in a current source inverter is a condition that must be avoided. This is because these conditions will produce a high voltage which can damage the scaling component. Therefore, it is necessary to add an overlap to provide the outgoing switch (switch that has been active) when switching from the ON position to OFF so that there will be an overlap (overlap between the active switch and the active switch). This is to ensure that the switch to be active is ON when the outgoing switch is OFF.

In this study, overlap time variations were carried out on multilevel current source inverters. This variation is needed so that the influence of overlap time on CSI multilevel performance can be analyzed. In addition, in this study we will explain how to minimize the negative effects caused by the addition of overlap time in multilevel CSI. In overlap time testing, multilevel CSI is given overlap time variations from 0 us to 5 us. In this test it was found that the greater the overlap time used, the greater the THD value of the inverter output current.

As for minimizing the negative effects of overlapping time, an overlap time compensation is given. There are 2 basic methods as compensation, namely using the total carrier triangle and using half of the total carrier triangle. In addition, the second method is used but with a phase difference between triangles of 180. At each of the lower peaks of the triangle, extended according to the amount of compensation. So that the bottom peak of the triangle passes through the original DC offset and crosses over the triangle below it. From the methods used, the method by using half of the triangular total carrier is very effective in minimizing the negative effects of overlapping time, which can reduce the THD value of the output inverter wave

Keywords : Overlap Time, Current Source Inverter Multilevel, Open Circuit